Harmonic-Balance Analysis of Digital Frequency Dividers

A. Anakabe, J. P. Pascual, J. Portilla, J. Jugo, and J. M. Collantes

***Abstract*—In this letter, a novel technique that enables the simulation of digital frequency dividers at low computation cost using conventional harmonic-balance software is presented. It relies on a continuation method, implemented with standard library elements, which is externally coupled to the core of the harmonic-balance algorithm. The technique provides a straightforward method for tracing solution curves and input sensitivity curves of frequency dividers. A digital divide-by-two monolithic microwave integrated circuit (MMIC) has been analyzed using the proposed technique.**

***Index Terms*—Frequency division, harmonic-balance simulation, nonlinear circuit analysis.**

I. Introduction

SIMULATION of frequency divisions is not an easy task for conventional harmonic-balance (HB) algorithms [1]. However, microwave designers can have important reasons for simulating frequency dividers with HB tools (either because time-domain simulations are not possible or are too time consuming, or because joint simulations with other high frequency circuits are required for noise analysis [2], etc.). Different techniques have been developed to assist designers in the HB simulation of frequency-divided steady states [3], [4]. Nevertheless, many commercially available HB simulators still lack a solution for frequency-division analysis. Since the designer does not have access to the core of this kind of simulators, the techniques that are normally used are based on optimization procedures [5], whose global computation time can be excessively long when applied to large circuits.

Here, a different technique is proposed to help standard HB algorithm to converge to the frequency-divided steady-state solution (when this solution does exist) at a lower computational cost. It is based on a nontrivial initialization of the frequency-divided components in the Fourier basis, coupled to a continuation method externally implemented to the HB core. Only standard library elements are required to implement the technique, which facilitates its application within commercial HB tools.

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A. Anakabe, J. Portilla, J. Jugo, and J. M. Collantes are with the Electricity and Electronics Department. University of the Basque Country, Bilbao, Spain (e-mail: jmcollan@we.lc.ehu.es).

J. P. Pascual is with the Department of Communication Engineering, University of Cantabria, Cantabria, Spain.

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II. Analysis Method

The frequency-division analysis is carried out using an auxiliary subharmonic circuit (ASC). The ASC serves to initialize the subharmonic frequency component of the circuit variables to nonzero values and permits the application of the continuation method. It is made up of three standard library elements connected in series:

- An independent voltage source with an operating frequency f_{ASC} corresponding to the subharmonic frequency component. In the case of division by two, f_{ASC} is equal to $f_0/2$, with f_0 being the external input frequency. Arbitrary values of amplitude, A_{ASC}, and phase, ϕ_{ASC}, are assigned to this voltage source. However, A_{ASC} must be different from zero in order to ensure the initialization of the subharmonic component to a nontrivial value.
- An ideal band-pass filter at f_{ASC}. In this way, the ASC only has an influence over the original circuit at its own operating frequency f_{ASC}.
- A resistance R_{VAR} whose value is variable. R_{VAR} acts as a continuation parameter playing a key role in the convergence process toward the frequency-divided solution and in the direct tracing of the solution curves.

The technique is illustrated by its application to a source coupled FET logic (SCFL) divide-by-two circuit intended to be part of a phase-locked VCO of a GaAs integrated transceiver. It consists of a master–slave D-type flip-flop with feedback from the inverted output to the data input (Fig. 1). The whole circuit (including buffers) contains 12 enhancement MESFETs, 16 depletion MESFETs, and six dc-shift diodes.

A. Convergence to a Frequency-Divided Steady-State Solution

In order to obtain the circuit steady-state response corresponding to a particular operating condition, the ASC has to be connected at a relevant node of the circuit. Output nodes prior to the buffering stages are the most suitable. In the case of the circuit under study, the ASC has been connected in parallel between the inverted and noninverted outputs (Fig. 1).

With the ASC connected to the circuit, a HB simulation is performed sweeping the continuation parameter R_{VAR} from very low to very high values (10^{-1} to $10^{10}\ \Omega$, for instance). In this simulation, each solution of the sweep is obtained using the previous solution as starting point. For low R_{VAR} values in the sweep, the solution provided by HB has necessarily nonzero values at the divided-frequency components ($f_0/2$), forced by the ASC. Obviously, these solutions are not yet the correct

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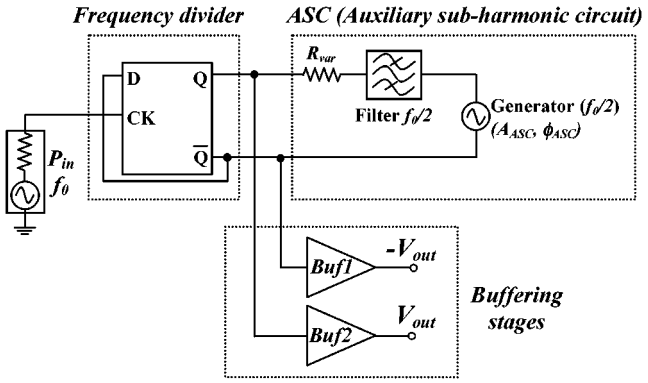


Fig. 1. Digital $\frac{1}{2}$-frequency divider based on a D-type flip-flop with the auxiliary subharmonic circuit (ASC) connected to its output.

steady-state response but they initialize the subharmonic components to nonzero values. As $R_{\rm VAR}$ increases the ASC has a smaller influence on the circuit response. Actually, for the largest values of $R_{\rm VAR}$ in the sweep, the ASC is open-circuited and has no effect at all on the circuit behavior, as in any standard continuation method.

Let us consider first an operating condition in which the circuit does not exhibit frequency division ($P_{in} = -22.6$ dBm, $f_0 = 3.2$ GHz). In this case, as $R_{\rm VAR}$ increases in the sweep, the solutions provided by HB tend progressively to the trivial solution without frequency-divided components. Actually, for the largest values of $R_{\rm VAR}$, the solution coincides with the steady-state response obtained from a standard HB simulation. This convergence process is illustrated in Fig. 2(a), in which the evolution of the frequency-divided component of the output voltage has been plotted, in magnitude and phase, versus the sweeping parameter $R_{\rm VAR}$. This convergence to zero is achieved for any arbitrarily chosen values of amplitude, $A_{\rm ASC}$, and phase, $\phi_{\rm ASC}$, of the ASC.

Let us consider now a circuit operating condition involving frequency division ($P_{in} = -16$ dBm and $f_0 = 3.5$ GHz). The sweep of the continuation parameter $R_{\rm VAR}$ results now in a smooth transition from an arbitrary frequency-divided solution (corresponding to the lowest value of $R_{\rm VAR}$) to a final frequency-divided solution (corresponding to the largest values of $R_{\rm VAR}$), as it is shown in Fig. 2(b). This final solution represents an actual solution of the circuit since it is achieved when $R_{\rm VAR}$ becomes large enough to prevent any influence of the ASC over the circuit. The input and output time waveforms corresponding to the last $R_{\rm VAR}$ value are plotted in Fig. 3(a). The input and output waveforms have been measured for the same operating condition using a microwave transition analyzer [Fig. 3(b)]. The good agreement confirms the validity of the HB results.

Three remarks need to be pointed out concerning the application of the technique.

i) The sweep of the continuation parameter $R_{\rm VAR}$ is logarithmic. Only one point per decade is required to achieve convergence to the actual frequency-divided solution, which reduces significantly the computation cost.

ii) When more than one frequency divided solution co-exist for a particular operating condition, these can be obtained by selecting different departing values for $A_{\rm ASC}$ and $\phi_{\rm ASC}$.

iii) Convergence toward a frequency divided steady state does not ensure the physical existence of that state. Therefore, any obtained frequency divided solution requires a large-signal stability analysis to guarantee its existence.

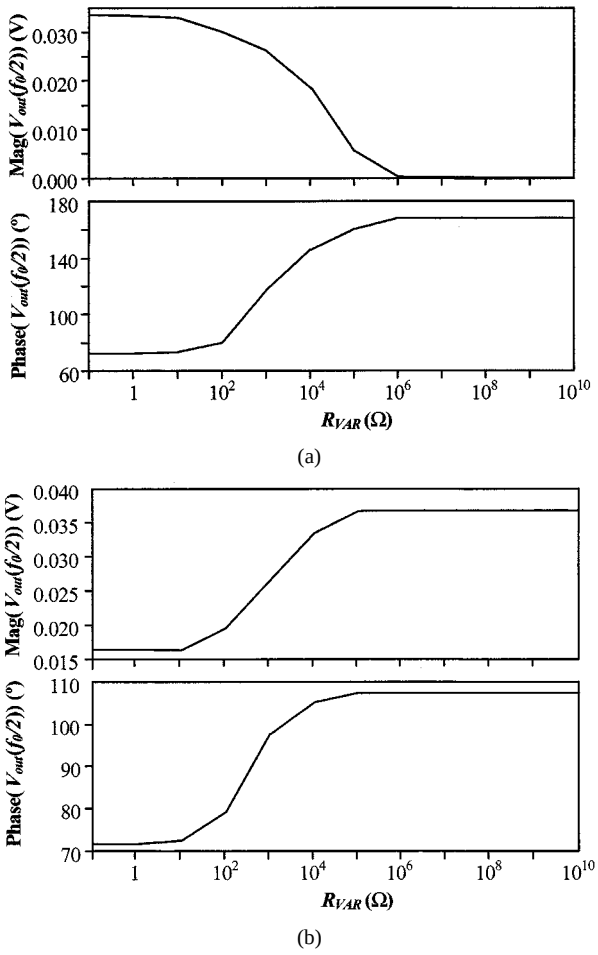
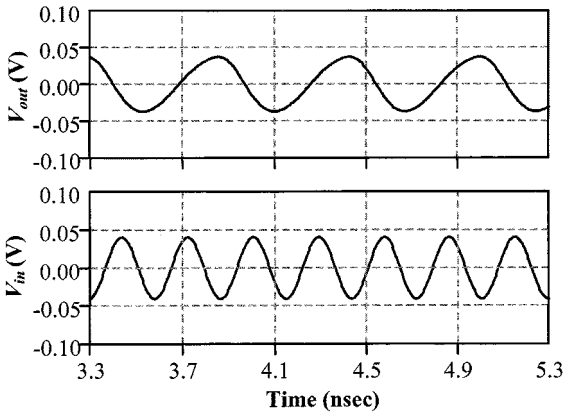


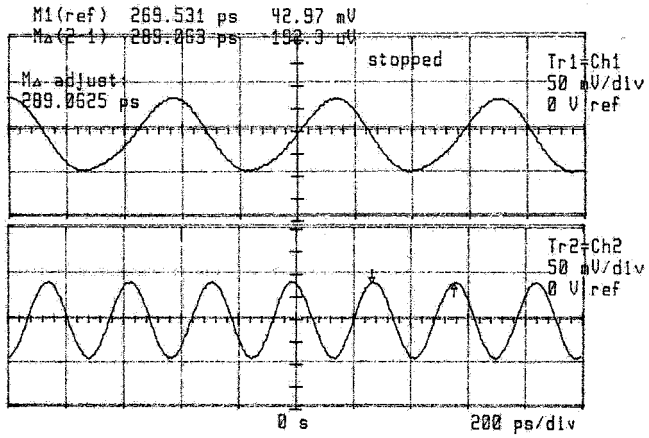
Fig. 2. Frequency-divided component of output voltage. Evolution of magnitude and phase as $R_{\rm VAR}$ is swept from 10^{-1} to 10^{10} Ω ($A_{\rm ASC} = 0.2$ V, $\phi_{\rm ASC} = -100°$). (a) $P_{in} = -22.6$ dBm at $f_0 = 3.2$ GHz. (b) $P_{in} = -16$ dBm at $f_0 = 3.5$ GHz.

B. Tracing of Solution Curves

The circuit solution curves versus any given circuit parameter can be obtained by simply performing a double sweep in $R_{\rm VAR}$ and the chosen circuit parameter. This must be a hierarchical sweep, in which the whole range of $R_{\rm VAR}$ is swept for each value of the circuit parameter. Then, the solution curve can be drawn by just plotting the value of the frequency-divided component (for the last value of the sweep in $R_{\rm VAR}$) versus the circuit parameter. In Fig. 4, the magnitude of the frequency-divided component ($f_0/2$) of the output voltage has been traced as a function of the input power for a constant input frequency $f_0 = 3.2$ GHz. It can be observed how the bifurcation leading to the frequency division takes place for $P_{in} \approx -22.2$ dBm. Although for these particular conditions frequency division is achieved by harmonic synchronization, solution curves corre-



(a)



(b)

Fig. 3. (a) Simulated output and input time waveforms for $P_{in} = -16$ dBm, $f_0 = 3.5$ GHz corresponding to the last $R_{\rm VAR}$ value. (b) Measured output and input time waveforms for $P_{in} = -16$ dBm, $f_0 = 3.5$ GHz.

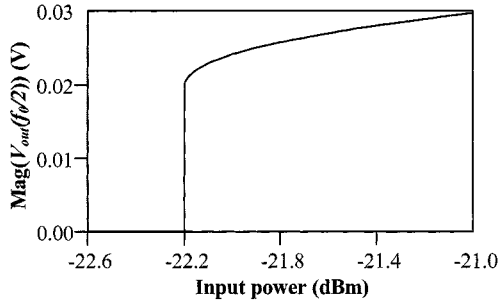


Fig. 4. Solution curve representing the magnitude of the frequency-divided component of output voltage versus input power for constant input frequency $f_0 = 3.2$ GHz.

sponding to I-type bifurcations can also be traced with the same procedure.

C. Tracing of Sensitivity Curves

The input sensitivity curve of a frequency divider is the bifurcation loci as a function of input power and frequency. Thus, the bifurcation points obtained from the solution curves at different input frequencies determine the input sensitivity curve. The input sensitivity versus input frequency of the circuit under study, obtained through the proposed technique, is shown in Fig. 5 with solid lines. Measurements have been superimposed with crosses in Fig. 5, showing reasonable agreement considering the complexity of the circuit. Due to its simplicity and relatively low computation cost, this analysis method can be employed to carry out robustness evaluation of the design by studying the effect of the dispersion of sensitive technological parameters. As an example, the input sensitivity curves corresponding to minimum and maximum values of the FETs intrinsic capacitances have been superimposed in Fig. 5 with dotted and dashed lines, respectively.

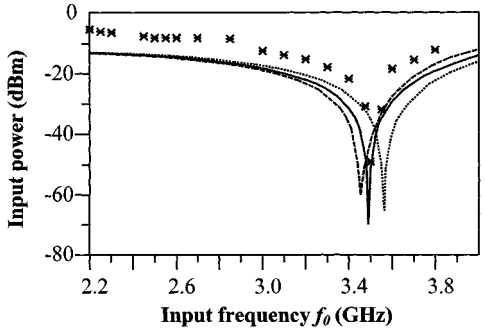


Fig. 5. Input sensitivity curve. *Solid line*: harmonic-balance simulation with actual values of FETs intrinsic capacitances; *dotted line*: harmonic-balance simulation with minimum values of intrinsic capacitances.; *dashed line*: harmonic-balance simulation with maximum values of intrinsic capacitances; *crosses*: measurements.

III. Conclusion

A technique for the analysis and design of digital frequency dividers in harmonic-balance simulators has been presented. The technique can be easily implemented in any commercially available HB software since it only makes use of standard library elements. Its relatively low computation cost, together with a straightforward tracing of solution curves, can help to reduce the design development cycles of high-frequency digital frequency dividers.

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